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STUDIES ON RELAXATION MECHANISM IN FIELD EFFECT TRANSISTOR

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ABSTRACT

In this work the field effect transistor BFW11 has been chosen for the study. The high frequency pertur-bations, were applied between the gate and the source in the range 10 MHz to 30 MHz in small regular steps. The corresponding losses and electrode capacitances were measured using an-accurate Q -meter. The real and imagi-nary components of the dielectric material silicon of the FET forming the capacitor were evaluated. The graph between the frequency and the real and imaginary components of the dielectric were obtained. Using Debye's dispersion relation the relaxation times for the Carriers were obtained.

KEYWORD : Electrode Capacitance, Dielectric material, Relaxation times, imaginary component, Frequency perturbations.

INTRODUCTION:

Field effect transistor is a unipolar device as its action depends upon only one type of charge carriers i.e., either electrons or holes. They are simple to fabricate and occupies less space in integrated form. Further a field effect transistor exhibits a high input resistance and are less noisy. Further the FET constants e.g., pinch-off voltage and the Channel width profile vary at such frequencies in addition to its parameters μ, r_d and g_m. Hence a thorough investigation at high frequencies is important. /1, 2, 3/

EXPERIMENTAL TECHNIQUE:

A field effect transistor BFW 11 was chosen for the present investigation. A Q-meter EE-13 was taken for the purpose of the measurement of the loss factor and capacitance between the two FET electrodes, the source and the gate. The necessary bias was applied between the gate and the source. Further the drain current was kept fixed for one complete set of frequencies i.e., in the range 10 to 30MHz. The drain currents were 0.1 m A, 0.3 m A, 0.5 m A and 0.7 m A. Initial reading without any application of the drain current was taken in the beginning, a pause of about five minutes was observed for the measurements of both the capacitance and the loss factor in all the readings so as to ensure the equilibrium effects of the majority carriers of the device. The real and imaginary components of the complex permittivity of the silicon material between the source and the gate were computed using the relations /2,3/

$$€' = \frac{1}{C_0} \frac{C_{obs}}{1+(\tan\delta)^2} - C_{cable} \qquad \ldots\ldots\ldots\ldots(1)$$

$$€'' = \frac{1}{C_0} \frac{C_{obs} \, . \, \tan\delta}{1+(\tan\delta)^2} \qquad \ldots\ldots\ldots\ldots(2)$$

$$\tan\delta = \tan\delta' - \tan\delta'' \qquad \ldots\ldots\ldots\ldots(3)$$

$$\tan\delta' = \frac{C}{C_1 - C_2} \left[\frac{1}{Q_1} - \frac{1}{Q_2}\right] \qquad \ldots\ldots\ldots\ldots(4)$$

$$\tan\delta'' = \frac{C_3}{C_3 - C_4} \left[\frac{1}{Q_3} - \frac{1}{Q_4}\right] \qquad \ldots\ldots\ldots\ldots(5)$$

where C_{obs} is the capacitance between the gate and source with doped silicon in the dielectric medium C_{cable} the capacitance of high frequency cable, C_0 the capacitance between electrodes without dielectric, $\tan\delta$ the loss factor of capacitor; $\tan\delta'$ the loss factor of capacitor between gate and source electrodes with doped silicon plus high frequency cable; $\tan\delta''$ the loss factor of high frequency cable; Q_1, C_1 and Q_2, C_2 are the Q-factors and capacitances observed respectively with and without silicon sample and Q_3, C_3 and Q_4, C_4 are the Q factors and capacitances observed respectively with and without the high frequency cable. Capacitor's loss tangent is stated as its dissipation factor or the reciprocals of its quality factor Q as follows :

Dissipation Factor $\tan\delta = \frac{1}{Q}$

Loss tangent can be calculated $\tan\delta = \frac{€''}{€}$

Result and Discussions:

The real and imaginary components of the complex permittivity of the doped silicon material are connected by the relation./4/

$$€* = €' - j\,€'' \qquad \ldots\ldots\ldots\ldots(6)$$

where € is the complex permitivity, €′ the real and €′′ the imaginary components of the complex dielectric constant. The applied field is of sufficiently low – frequency, the dipoles can follow the field completely and $€*$ takes on equilibrium value of $€_s$. When the frequency is high, the dipoles cannot follow the field reversed, and

$€*$ takes an instantaneous value of $€\infty$. The calculated values for C_o €′ and C_o €″ versus frequency are plotted in figures 1 and 2 respectively. It is observed that the values of €′ is negative in the frequency range 10 MHZ to around 20 MHZ. This shows that the behaviour of the silicon sample in this frequency range is more or less comparable to plasma properties where dielectric reduces below unity. The behaviour like plasma may be attributed to the fact that instead of two types of carriers as in the case of the ordinary bipolar transistor, the FET consists of only one type of carriers - the majority carriers only. Further the majority carriers in such materials used for the fabrication of the device is the only dopant; and as such the charge neutrility is maintained in the material and the atoms of intrinsic silicon and the impurity farms a plasma like behaviour specially at high frequencies. Further at high frequencies the equilibrium is obtained after the application of the electromagnetic wave to these atoms. Hence a dielectric relaxation is obtained. From second graph one finds that the dielectric relaxation is obtained corresponding to the frequencies in the range of 15 MHz to 20 MHz. This give the relaxation time. /5/

$$\tau = \frac{1}{\omega}$$

$$= \frac{1}{2\,\pi f}$$

$$= \frac{1}{2*3.14*15*10^{6}}$$

= 10 n Sec. or 8 n Sec. (approx)

such values of the relaxation time are in agreement with the theoretical predicted values.

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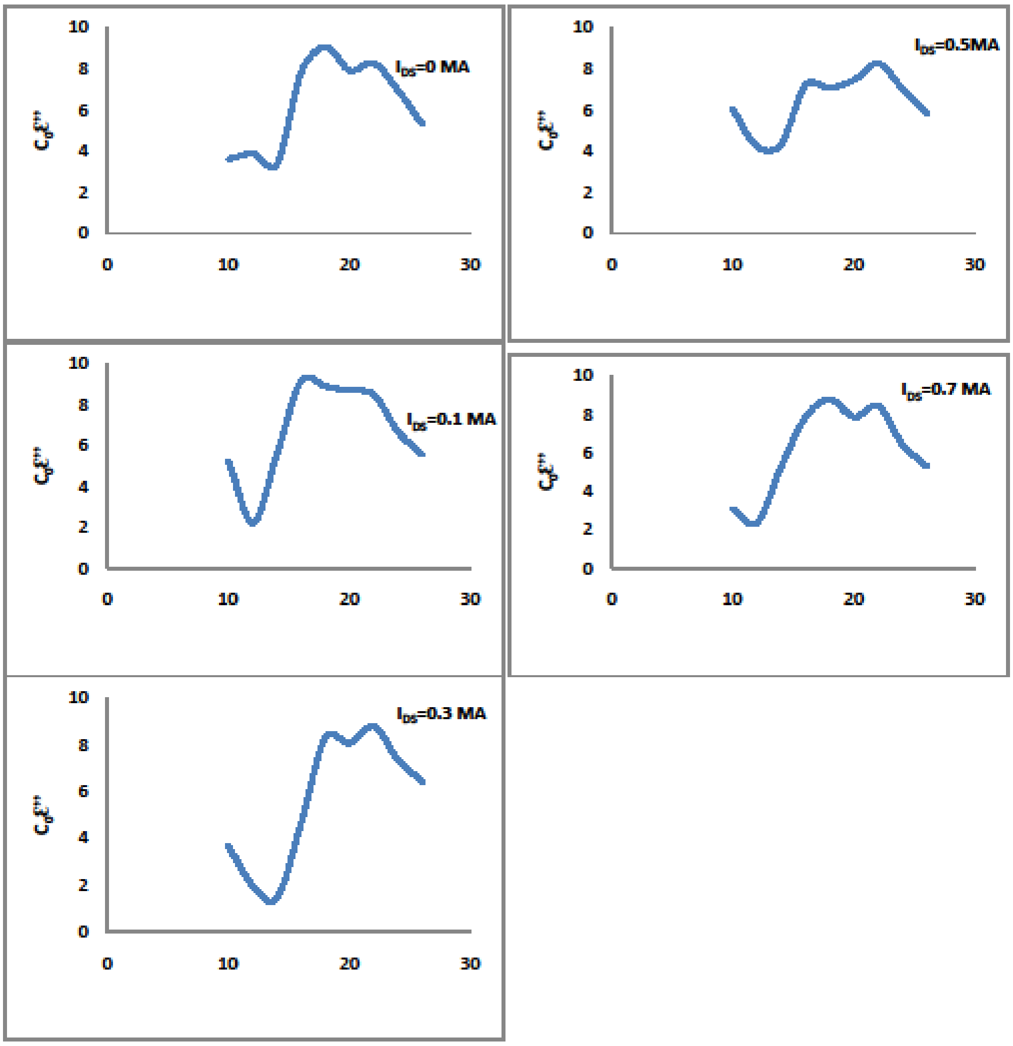
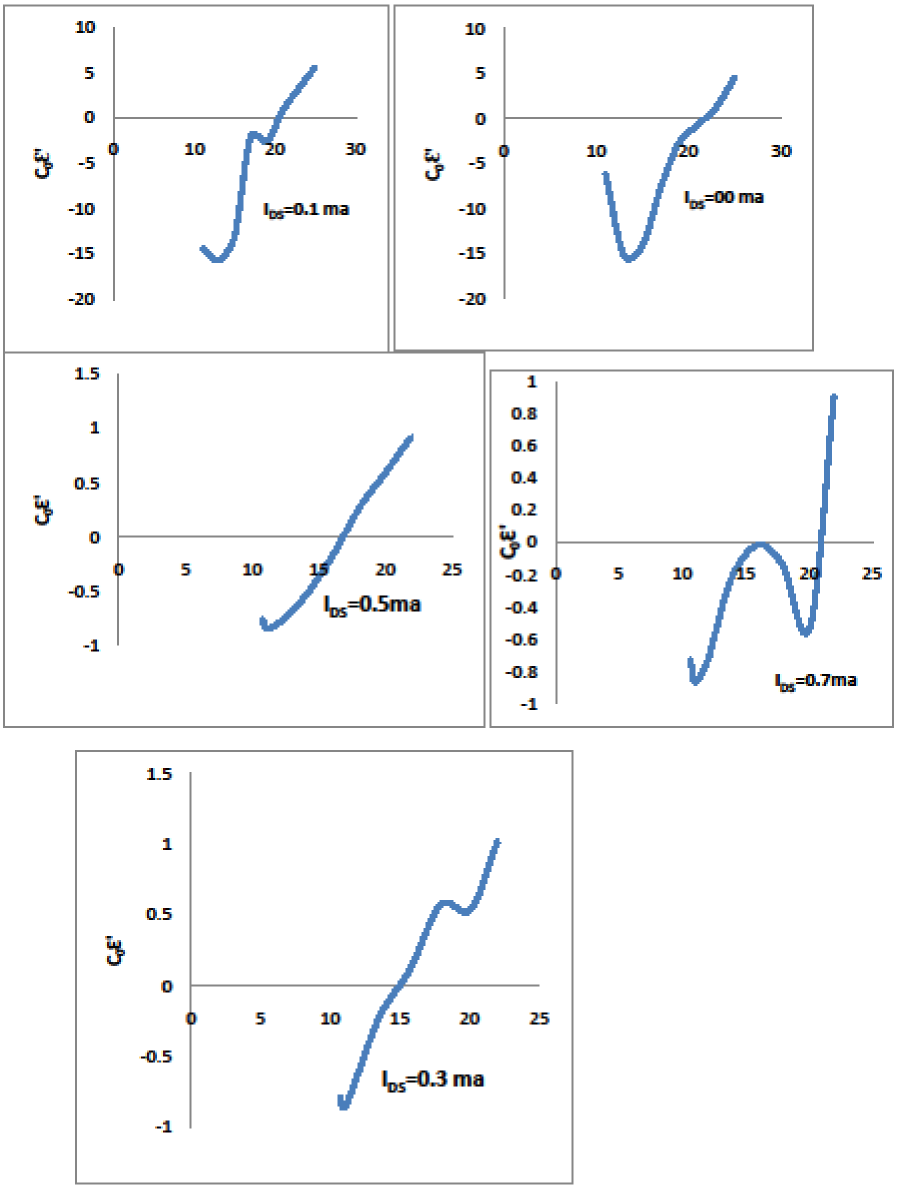


FIG $C_0\varepsilon''$ VERSUS FREQUENCY FOR BFW 11



$C_0\varepsilon'$ Versus Frequency for FET BFW 11