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A STUDY OF SIGMA-DELTA MODULATOR PERFORMANCE FOR AUDIO APPLICATION

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Abstract :

Analog to Digital converters fined different usage in various receiver design architectures. Analog modules appear to be precise and quite resistant to a variety of sources of noise and interference. Most of the highly precise A/D converters involve the use of sigma-delta modulation which is associated with over sampling and noise shaping. These converters use the least parasitic capacitances and small feature sizes characteristic of scaled VLSI technology by trading speed for resolution.

Keywords– Analog-to-digital converter, Sigma Delta modulation, over sampling

Introduction:

There is huge demand in the wired, wireless communication in day to day life for larger bandwidths and operating at high performance. Analog to Digital Converters is the applications for low power dissipation. Very high speed, low noise and less Offset voltage are requirements for mobile and portable devices. Analog to Digital Converter provides the bridge which links the analog world and the digital world. It converts the analog signal to the digital signal, and facilitates for the storage, processing and transmission of the data. The ADCs are generally categorized as Nyquist rate ADCs and Over sampling ADCs. These classifications are based on the rate at which the signal is sampled relative to the signal bandwidth. Complex and precise analog components are replaced by digital signal processing techniques in over sampling converters. A scope to achieve much higher resolution is provided by

this than Nyquistrate converters. Sigma Delta ADC, a over sampling type ADC is highly tolerant to analog circuit imperfections, thus providing it a one of the best choice to realize embedded ADC interfaces in modern systems on chip [1, 2]. It has been accepted as choice for audio and video processing system, medical imaging, and modern voice band and high resolution industrial measurement application. The Sigma Delta (ΣΔ) ADC is now used for noise shaping at high resolution applications. The method in which high-resolution signals are encoded into lower resolution signals using pulse density modulation is called as Sigma Delta modulation. Using DT, Discrete Time, and CT, Continuous Time, techniques Delta-Sigma modulator can be implemented which is one of the key building blocks. Compared to their DT counter parts, much attention have been attracted by CT Delta-Sigma modulators due to their advantages in terms of high resolution, operate at higher sampling rate, reduces the power consumption, low noise, high speed and intrinsic antialiasing capability [3].

Single-loop topologies:

Single-Loop versus Cascade Sigma-delta modulators. Sigma-delta Modulators employing only one quantizer are called single-loop topologies, whereas those using several quantizers are often named cascade or Mash Sigmadelta Modulators.

1. Single-Bit versus Multibit Sigma-delta Modulators which is attending to the number of bits in the embedded quantizer.

2. Low-Pass versus Band-Pass Sigma-delta Modulators which is attending to the nature of the signals being converted.

Discrete-Time versus Continuous :

Time Sigma delta Modulators which is attending to the nature of loop filter dynamics. In Sigma-delta Modulators the DT loop filter is used. However, in practice CT Sigma-delta Modulators can also be implemented. According to this classification criteria another type of sigma-delta modulators, known as hybrid CT/DT Sigma-delta Modulators take advantage of the benefits of both DT and CT implementations.

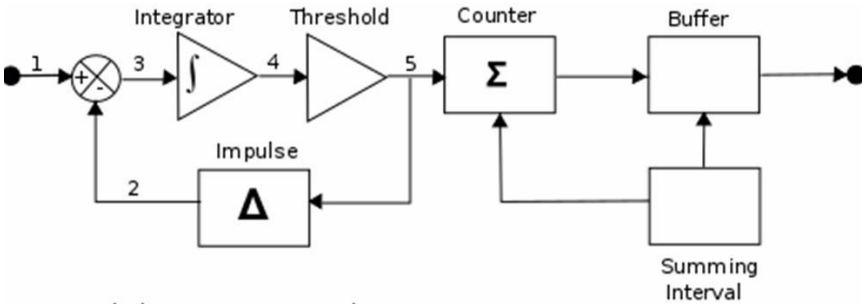

FIG. 1. Block diagram of sigma delta ADC

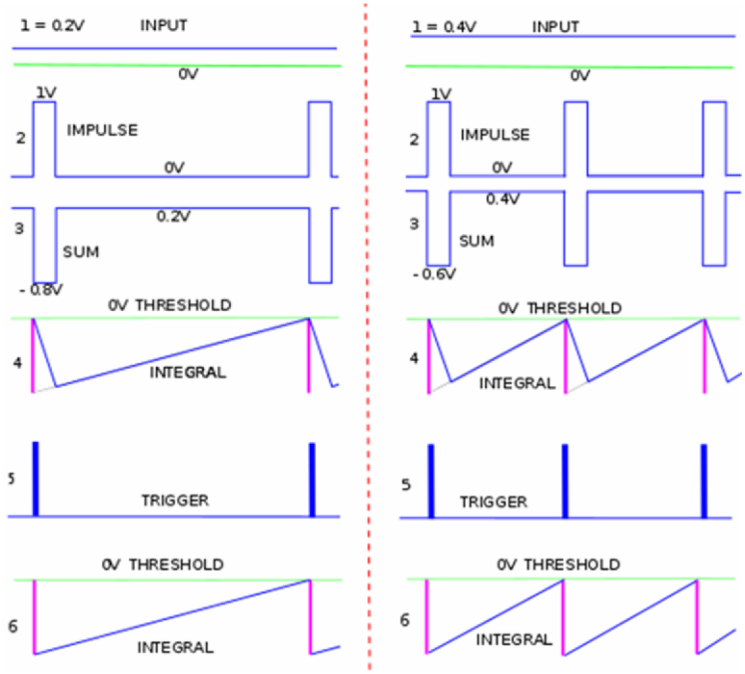

Fig. 2 Typical wave forms

Block diagram and waveforms for a sigma delta ADC is shown in FIG. no. 1 and 2 given above. The waveforms are denoted at points designated by numbers 1 to 5 for an input of 0.2 volts on the left and 0.4 volts on the right. In most practical applications the summing interval is large compared with the impulse duration and for signals which are a significant fraction of full scale the variable separating interval is also small compared with the summing interval. The Nyquist Shannon sampling theorem requires two samples to render a varying input signal. The samples appropriate to this criterion are two successive Σ counts taken in two successive summing intervals. The summing interval, which must accommodate a large count in order to achieve adequate precision, is inevitably long so that the converter can only render relatively low frequencies. Hence it is convenient and fair to represent the input voltage (1) as constant over a few impulses. Consider first the closed feedback loop consisting of the analogue adder/ subtracter, the integrator, the threshold crossing detector and the impulse generator. On the left 1 is the input and for this short interval is constant at 0.2 V. The stream of delta impulses generated at each threshold crossing is shown at 2 and the difference between 1 and 2 is shown at 3. This difference is integrated to produce the waveform 4. The threshold detector generates a pulse 5 which starts as the waveform 4 crosses the threshold and is sustained until the waveform 4 falls below the threshold. Within the loop 5 triggers the impulse generator to produce a fixed strength impulse. On the right the input is now 0.4 V and the sum during the impulse is −0.6 V as opposed to −0.8 V on the left. Thus the negative slope during the impulse is lower on the right than on the left. Also the sum is 0.4 V on the right during the interval as opposed to 0.2 V on the left. Thus the positive slope outside the impulse is higher on the right than on the left. The resultant effect is that the integral (4) crosses the threshold more quickly on the right than on the left. A full analysis would show that in fact the interval between threshold crossings on the right is half that on the left. Thus the frequency of impulses is doubled. Hence the count increments at twice the speed on the right to that on the left which is consistent with the input voltage being doubled. The overall effect of the negative feedback loop is to maintain the running integral of the impulse train equal to within one impulse to the running integral of the input analogue signal. Also the frequency of the impulse train is proportional to the bandwidth limited amplitude of the input signal. Bandwidth limitation occurs because the Nyquist–Shannon sampling theorem requires 2 impulses per period to define the highest frequency passed.

Construction of the waveforms illustrated at (4) is aided by

concepts associated with the Dirac delta function in that all impulses of the same strength produce the same step when integrated, by definition. Then (4) is constructed using an intermediate step (6) in which each integrated impulse is represented by a step of the assigned strength which decays to zero at the rate determined by the input voltage. The effect of the finite duration of the impulse is constructed in (4) by drawing a line from the base of the impulse step at zero volts to intersect the decay line from (6) at the full duration of the impulse.

Switched capacitor integrator:

Alireza Nilchi[4]has presented, a low power switched capacitor integrator based on a capacitive charge pump. The CP integrator is used as the first stage of sigma delta ADC. The 10kHz BW of CP ADC achieves 87.8 dB SNDR, while consuming 148uW, The conventional ADC has similar performance but dissipates 241uW. The energy required per conversion step for the CP based ADC is almost 40% lower than that of the conventional ADC. As Compared to conventional ADC, the CP based modulator achieves the suited for sensory or wireless system with small inputs, where it can significantly reduce the power consumption of dominant front end circuits. Below Fig. 3 (a) shows conventional SC integrators & Fig. 3 (b) shows proposed CP integrators used in sigma delta modulators. Fig. 4. shows measured SNR and SNDR for the CP and conventional sigma delta modulators.

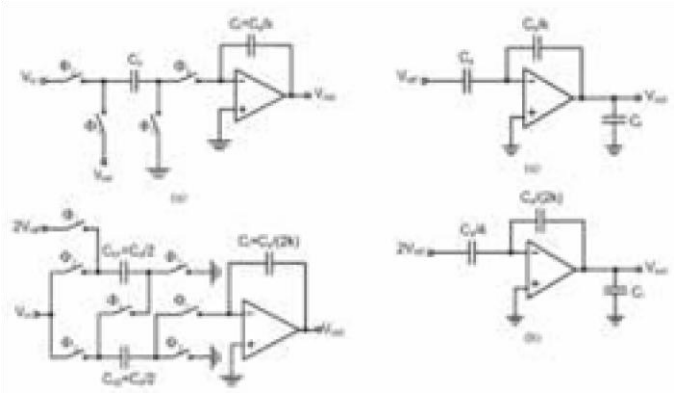

Fig. 3 (a) conventional SC integrator, (b) proposed CP integrator

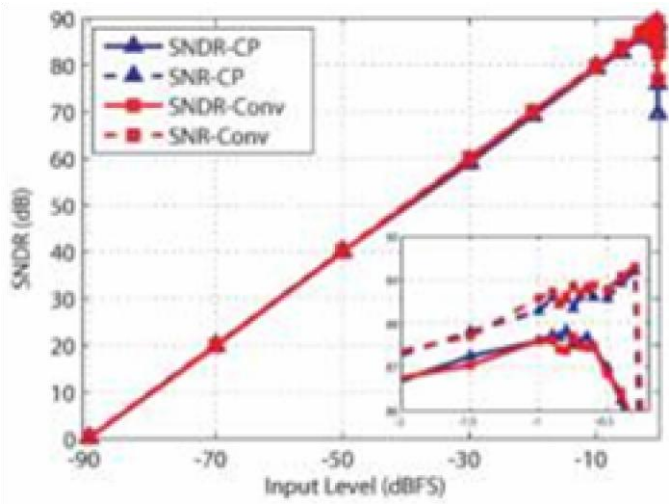

Fig.4. Measured SNR &SNDR versus i/p signal level for the CP and conventional ΣΔ modulators

Discussion:

Sigma delta modulators are widely used in wired & wireless applications. This investigation incorporates Second order modulators efficiently exchange the high speeds of CMOS VLSI technology for high analog resolution, low power and audio application

without sacrificing modulator stability or placing severe constraints on the precision of the analog circuits. Besides requiring more complex and precise anti-aliasing filter.

Conclusion :

Sigma delta modulators are widely used in wired & wireless

applications. This paper incorporates Second-order modulators efficiently exchange the high speeds of CMOS VLSI technology for high analog resolution but Sigma-Delta Modulation technique can also we used for different application but this review paper present an overview to ADC using Sigma delta modulator, using this technique it is simple to perform the conversion, using a simple circuit.

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