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SIMULATION OF AN ASYMMETRIC CASCADED MULTI LEVEL INVERTER SYSTEM

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Abstract: The proposed work deals with simulation of an asymmetric cascaded seven level inverter fed induction motor drive system. Asymmetric cascaded seven level inverter fed induction motor drive system is simulated and the corresponding results are presented. FFT spectrums for the outputs are analyzed to study the reduction in Total Harmonic Distortion (THD) of the inverter system.

Keywords:THD, Induction motor, Multilevel inverter, Asymmetrical cascaded inverter, Matlab Simulink.

1. GENERAL

Inverter fed induction motor suffers from the presence of significant amount of harmonics which causes undesired motor heating, torque pulsation and electro-magnetic interference. In order to reduce the harmonics, large sized filters are needed, which results in larger size and increased cost of the system. However the advanced achievements in the field of industrial electronics and power electronics made possible to reduce the magnitude of harmonics using multilevel inverter structures.

Nowadays, in high voltage and high power motor drive applications, multilevel inverters are the cost effective solution and most promising alternative to achieve good quality of output power [5]. Using the Multilevel inverter structure the power handling capability of the system can be raised in a systematic and powerful way [6].

In multi level inverters, the number of output voltage and current waveforms are increased without increasing the size of the filter. The term multilevel starts with the three-level inverter introduced by Nabae et al [7]. By increasing the number of levels of the inverter, the output voltage waveform contains more steps generating a staircase waveform, which is implemented on a multi level inverter with DC sources. By applying this concept, specific harmonics can be eliminated and the output voltage Total Harmonic Distortion (THD) can be improved, thus generating a low distorted sinusoidal waveform.

2. SEVEN LEVEL INVERTERSYSTEM

Seven level inverter fed induction motor drive system uses Asymmetric Cascaded Multilevel Inverter (ACMLI) consisting of two cascaded H-bridge inverters: a main bridge inverter and an auxiliary bridge inverter. The load is connected in such a way that the sum of the outputs of these inverter bridges will appear across the load. The ratio of power supplies between the auxiliary bridge and main bridge is 1:2.

3.OPERATION OF ASYMMETRIC SEVEN LEVEL INVERTER

Asymmetric cascaded seven level inverter consists of two H-bridge inverters and the output phase voltage of the seven level inverter is synthesized by the sum of output voltages of the two H-bridges. The first H-bridge or main bridge H_1 consists of DC source of $1V_{dc}$, whereas the second H-bridge or auxiliary bridge H_2 consists of DC source of $2V_{dc}$. Each H-bridge can generate three different voltage outputs by appropriate opening and closing of its switches. The main bridge can generate $+2V_{dc}$, 0, $-2V_{dc}$ and the auxiliary bridge can generate $+V_{dc}$, 0, $-V_{dc.}$ By using proper combination of switching devices many voltage levels are obtained. When the positive group switches (S_1, S_4 for main bridge and S_5, S_8 for auxiliary bridge) are simultaneously turned on, the voltage across that particular bridge is positive. When the negative group switches ($S_{2,}$ S_3 for main bridge and $S_{6,}$ S_7 for auxiliary bridge) are simultaneously turned on, the voltage across that particular bridge is negative. When S_1 and S_4 are turned on, the voltage across the main bridge is $+2V_{dc}$. When the S_2 and S_3 are turned on, the voltage across the main bridge is $-2V_{dc}$. Similarly, when S_5 and S_8 are turned on, the voltage across the auxiliary bridge is $+V_{dc.}$ When S_6 and S_7 are turned on, the voltage across the auxiliary bridge is $-V_{dc.}$ To obtain $+3V_{dc}$ the combination of switches S_1, S_4, 5_5& S_8 must be turned on. To obtain $-3V_{dc}$ the combination of switches S_2, S_3, S_6 & S_7 must be turned on. By simultaneous turning of switches S_1, S_2 or $S_{3,}$ S_4 or $S_{5,}$ S_6 or S_7, S_8 results in zero output voltage. The output voltage of H_1 is taken as V_1 and the output voltage of H_2 is taken as V_2. The output voltage of seven level inverter is $V = V_1+V_{2.}$ Thus, the seven level inverter output voltage of $+3V_{dc}$, $+2V_{dc}$, $+1V_{dc}$, 0, $-V_{dc}$, $-2V_{dc}$, and $-3V_{dc}$ can be obtained. Table 1 shows the switching states of transistors, output voltage of H-bridges and the output voltage of seven level inverter. If the status of the switch is '0', that switch is in OFF position and if the status of the switch is '1', that switch is in ON position.

Table 1 Switching states of transistors of seven level inverter.

Voltage level	S_1	S_2	S_3	S_4	V_1	S_5	S_6	S_7	S_8	V_2	$V = V_1+V_2$
1	0	1	1	0	$-2V_{dc}$	0	1	1	0	$-1V_{dc}$	$-3V_{dc}$
2	0	1	1	0	$-2V_{dc}$	0	0	1	1	0	$-2V_{dc}$
3	0	0	1	1	0	0	1	1	0	$-1V_{dc}$	$-1V_{dc}$
4	0	0	1	1	0	0	0	1	1	0	0
5	0	0	1	1	0	1	0	0	1	$+1V_{dc}$	$+1V_{dc}$
6	1	0	0	1	$+2V_{dc}$	0	0	1	1	0	$+2V_{dc}$
7	1	0	0	1	$+2V_{dc}$	1	0	0	1	$+1V_{dc}$	$+3V_{dc}$

3. SIMULATION RESULTS OF SEVEN LEVEL INVERTER

The simulation is done using Matlab Simulink version 7.9 and the results are presented. The single phase structure of cascaded seven level inverter with resistive load is shown in Figure 1. It has two cascaded inverters: A main bridge inverter which has DC input voltage of 200 V and an auxiliary bridge inverter with input voltage of 100 V. Driving pulses for M_1 and M_2 are shown in Figure 2. The output voltage of main bridge is shown in Figure 3. The output voltage of auxiliary bridge is shown in Figure 4. The output voltage across the load of 7 level inverter is shown in Figure 5. It can be seen that the output has 7 levels. The output current is shown in Figure 6. The speed response of seven level inverter fed induction motor drive is shown in Figure 7. The speed increases and settles at 1410 rpm. FFT analysis is done for the output current as well as output voltage and the corresponding spectrums are shown in Figure 8 and 9 respectively. The current TD is 6.06 percent and voltage THD is 7.94 percent.

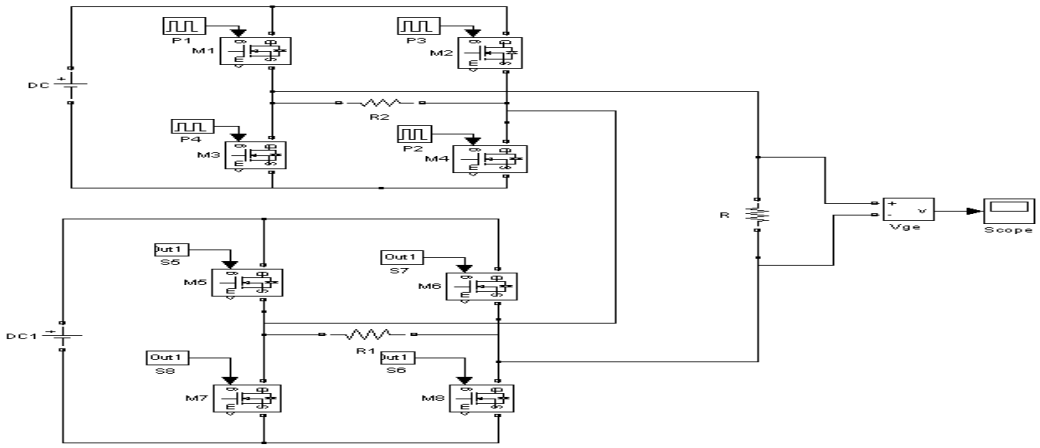

Figure 1. Single phase structure of seven level inverter

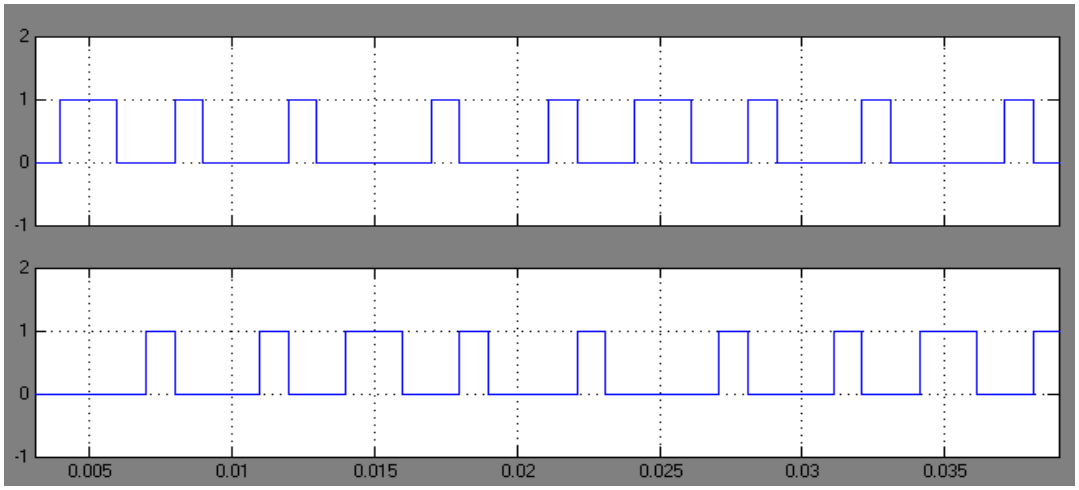

Figure 2. Driving pulses for M_1& M_2 of seven level inverter

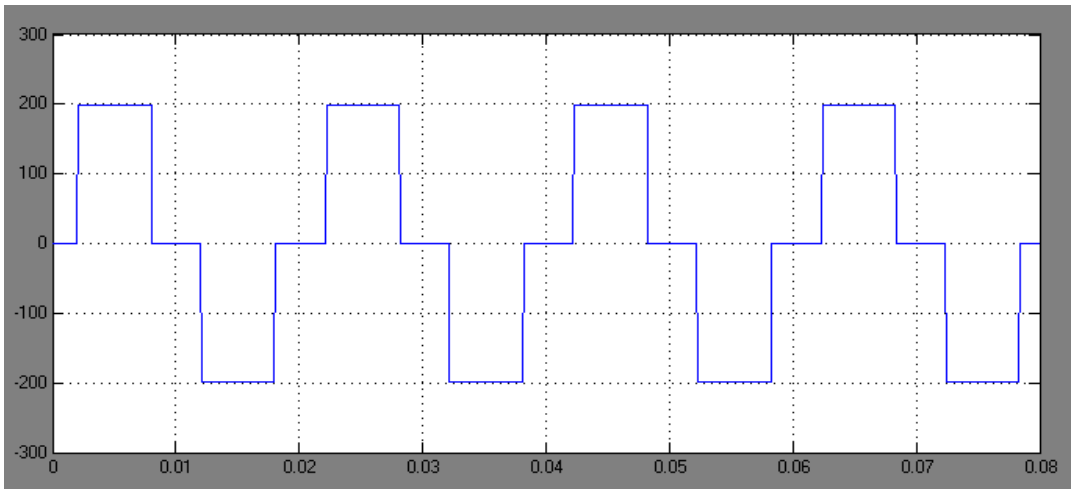

Figure 3. Output voltage of main bridge of seven level inverter

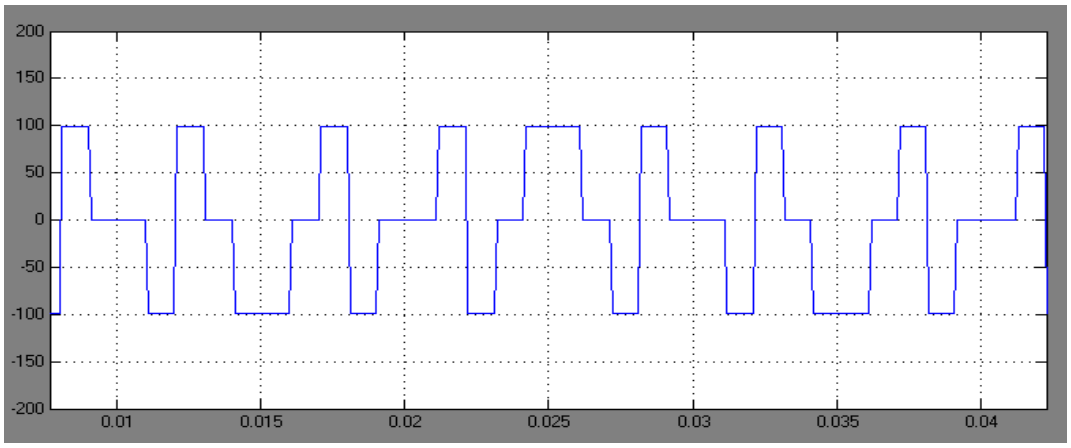

Figure 4 Output voltage of auxiliary bridge of seven level inverter

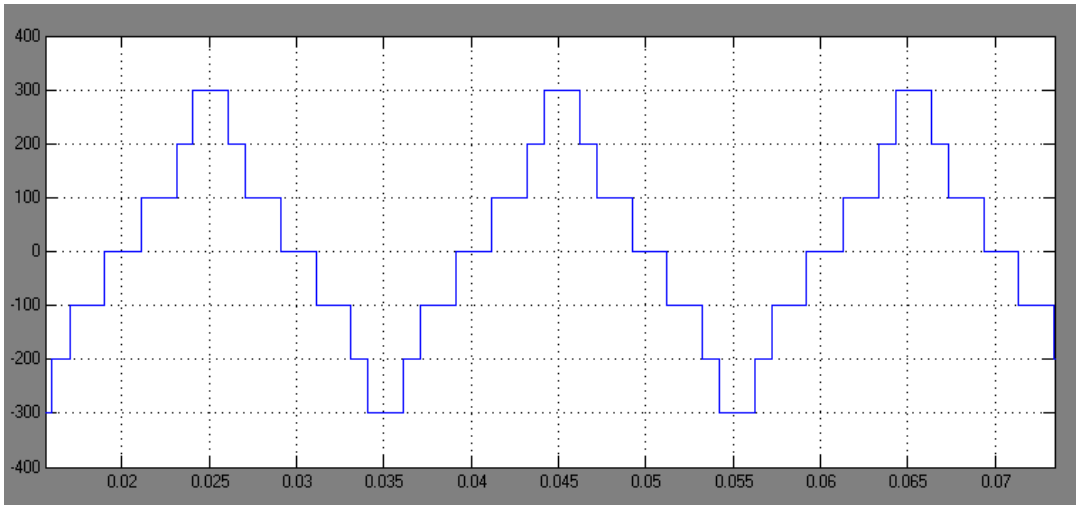

Figure 5. Output voltage of seven level inverter

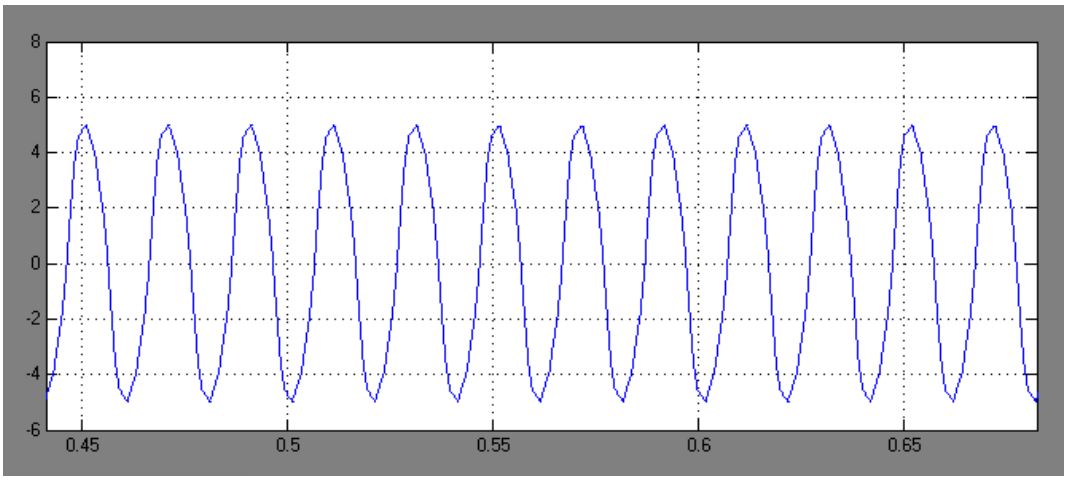

Figure 6. Output current of seven level inverter

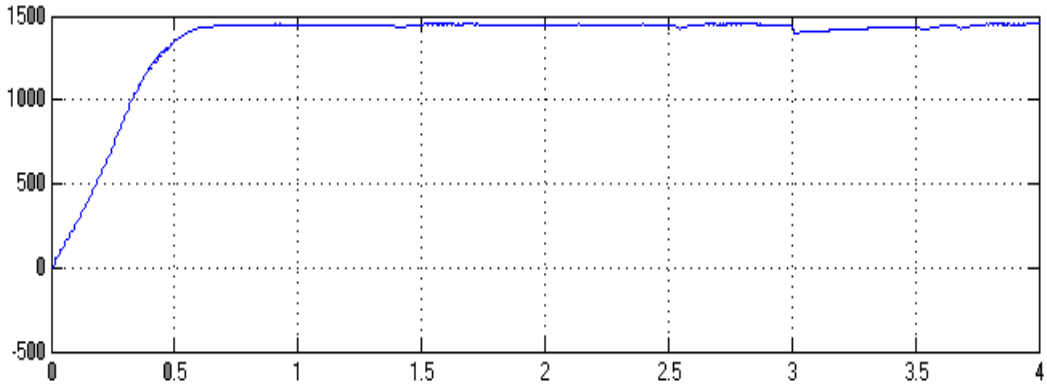

Figure 7. Rotor speed of seven level inverter fed IM drive

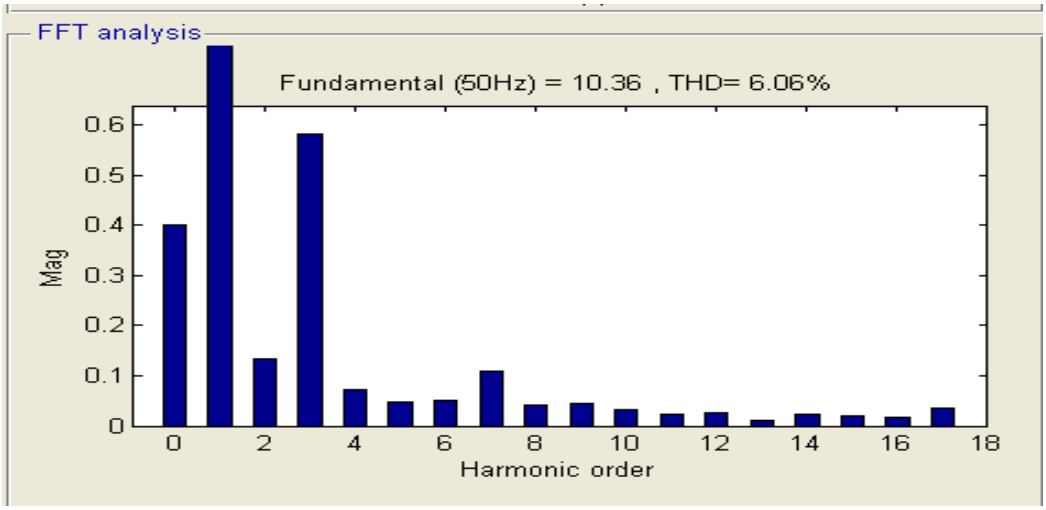

Figure 8. FFT spectrum for stator current of 7 level inverter

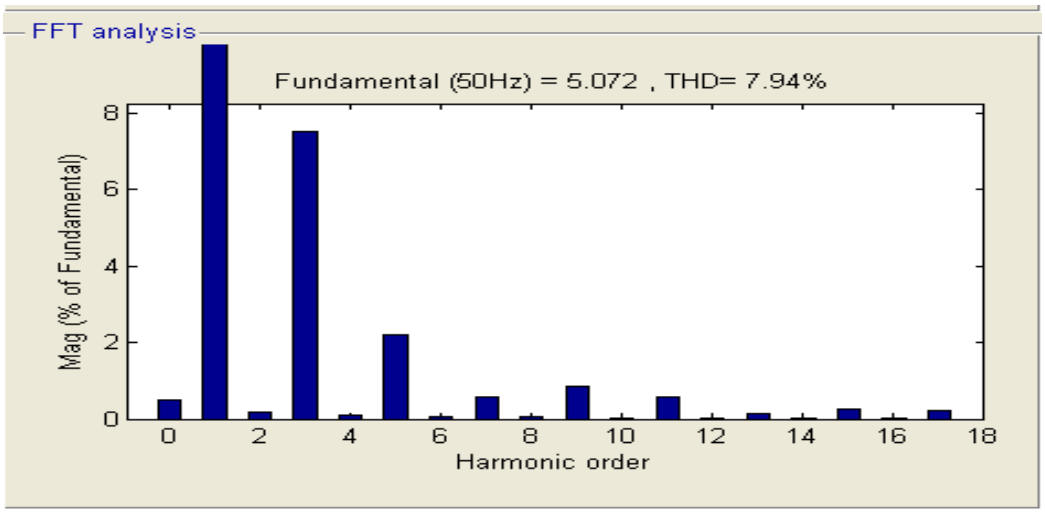

Figure 9. FFT spectrum for stator voltage of 7 level inverter

4. CONCLUSION

Seven level cascaded inverter fed induction motor drive system with unequal DC sources is simulated and the corresponding results for stator voltage, stator current, rotor speed are presented. FFT spectrums for the output current and output voltage of inverter system are also presented. The simulation results of current THD and voltage THD are 5.67 percent and 7.12 percent respectively. Rotor speed is 1410 rpm. It is concluded that the performance of seven level inverter system is better than the classical inverter system.

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