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CMOS DESIGN OF Ka-BAND POWER AMPLIFIER FOR SATELLITE APPLICATIONS

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ABSTRACT

Communication satellites make use of transponder to transmit and receive signals from respective earth stations. These transponders consist of Power Amplifier which is the last electronic component in it. They are used to amplify the power of the signal and make it available for driving the antennas. In this paper, a Ka-Band class AB PA is proposed using a cascaded topology. It is designed using CMOS technology to reduce chip area and power consumption.

KEYWORDS: Power Amplifier (PA), CMOS, efficiency, linearity, Class AB, Common-Source (CS).

1. INTRODUCTION

In a typical transmitter receiver system, PA is used to drive the antenna. It is very challenging to design this RF electronic component. Main trade-off exists between the required and the available voltage. While CMOS is a low voltage process, power amplifier needs a larger voltage swing to perfectly increase the power of the signal and hence make it available to the antenna for transmitting. It is obvious that the power level should be high enough, such that it is easier for the antenna to cover a wide area.

For the ease of operation, PAs are classified into various classes based on the mode of operation. These different classes almost have the same configurations; however, the biasing networks are different. Class A amplifier is the simplest power amplifier. The biasing is done in such a way that the amplifier conducts throughout the cycle and transistor always remains ON. Moreover, it shows the highest linearity and is quite stable with very low distortion level. The main drawback is the efficiency. As it remains ON most of the time, it shows a low efficiency of 50%. Hence, it is not used for high power applications.

Second is Class B amplifiers. These PAs conduct for only half cycle with a conducting angle of 180 degrees. They are also quite stable but have the advantage that they give out an efficiency of 75% or more. Though it's design is more efficient, it has a large area headroom as we need two different sets of transformers to amplify positive and negative half cycles. A Class AB power amplifier is the one

which remains on for more than half a cycle but less than a full cycle. It is a combination of Class A and B amplifiers. Its efficiency is also between them i.e. around 60-65%. It is one of the most used amplifiers in audio applications and receivers. Class C amplifiers on the other hand remain on for less than a half cycle thus conducting for an angle around 90 degrees. It is highly efficient (80%-90%) with a lower operating cycle but it has low linearity and high distortions due to which it is not that popular in industrial CMOS applications. Class D amplifiers are mostly used for pulse width modulation techniques.

Next section describes step by step design methodology for proposed class AB power amplifier.

2. DESIGN METHODOLOGY

To start with the design process for any electronic component firstly we need to set target performance of various parameters. In case of a PA, the most important performance parameters are efficiency and linearity. It needs to be ensured that the circuit is stable to achieve linearity. Unstable circuits often produce a non-linear output. If we consider our circuit in terms of a two port network then the stability criterion is as follows;

$$K = \frac{1 - |s_{11}|^2 - |s_{22}|^2 + |\Delta|^2}{2|s_{12}s_{21}|}$$

where,

$$\Delta = s_{11}s_{22} - s_{12}s_{21}$$

For the system to be stable the conditions to satisfy are;

$$K > 1$$

$$|\Delta| < 1$$

If these conditions are satisfied then the system is stable and should produce good linearity. The other main keyword in PA is efficiency. Efficiency is basically the ratio of consumed power to the delivered power.

$$\eta = \frac{P_{OUT}}{P_{SUPPLY}}$$

the above equation does not take into account the input power applied hence another metric should be defined. One such parameter is Power Added Efficiency (PAE). It is given as,

$$\eta_{PAE} = \frac{P_{OUT} - P_{IN}}{P_{SUPPLY}}$$

After taking into account these two parameters it is essential to choose the class of power amplifier for the intended application. Class AB is selected due to its ease of design, biasing condition and its higher efficiency. This will of course lead to trade-off between linearity and efficiency i.e. though class AB provides better efficiency than class A amplifier, at higher frequencies it does produce some non-linearity. Nonetheless, the nonlinear effects are tolerable and can be worked with.

Next step is to design the input and output matching networks to ensure maximum transfer of power (much more critical in case of a power amplifier). Input matching and the biasing network should be

designed in accordance with each other. An important fact that needs to be taken in account is that the biasing network should be such that the circuit conducts for more than half the duty cycle (since class AB is used). Moreover, bising network should be such that it does not interfere with the matching networks. For the input and output to be perfectly matched, the following condition must hold true; $Z_{in} = Z_{out.\ generally,}$ as an accepted norm the ports are matched at 50ohms.

After this comes the design of transistors and selection of a perfect topology. Following section discusses the proposed design and its analysis.

3. DESIGN OF POWER AMPLIFIER

Designing a RF CMOS power amplifier is a tedious task. When going for designing a analog electronic device, we firstly select the kind of topology and power requirements of the device. However in this case we first need to choose a class of PA (Class A or B etc.) after which we need to model the biasing and matching networks. A deep class AB amplifier is selected due to its good efficiency and performance. Now the biasing network is very important as it makes sure the device operates in the selected class of amplifiers. Class AB requires that the transistor should be ON for more than half the input cycle. Therefore the biasing should be such that it fulfills this condition. Matching network and biasing state should be designed simultaneously to compensate both input impedance matching and the power and biasing requirements.

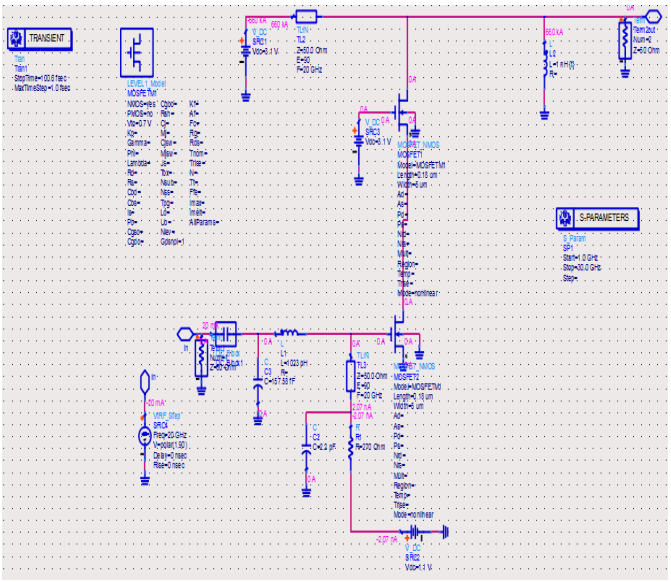

Figure 1

Above figure shows the schematic of proposed PA. The Power Amplifier has a cascode topology and it is of type Class-AB. Overall power supply is 3.1 V and the cascoded MOSFET's gate terminal is grounded. Hence it serves as a resistor or a load for the operating transistor. RF input source is selected with an input frequency of 18-19GHz. Parallel inductor-capacitor is used for input matching and another voltage source is present to maintain the bias on the transistor. Values of lumped parameters were optimized using ADS (Advanced Design System). Following figures show the gain of the amplifier and the magnitude of output gain.

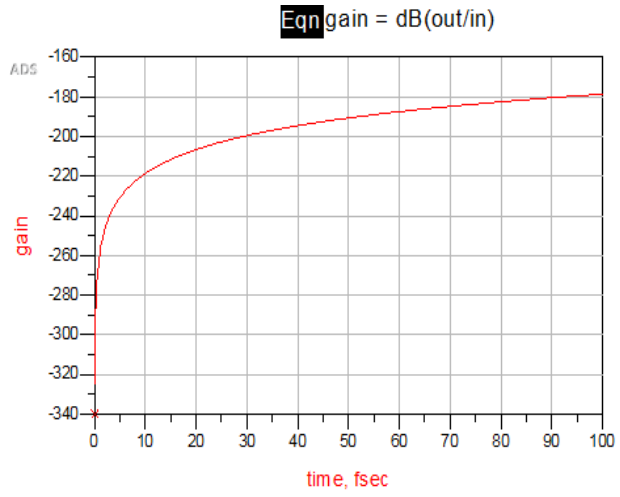

Figure 2

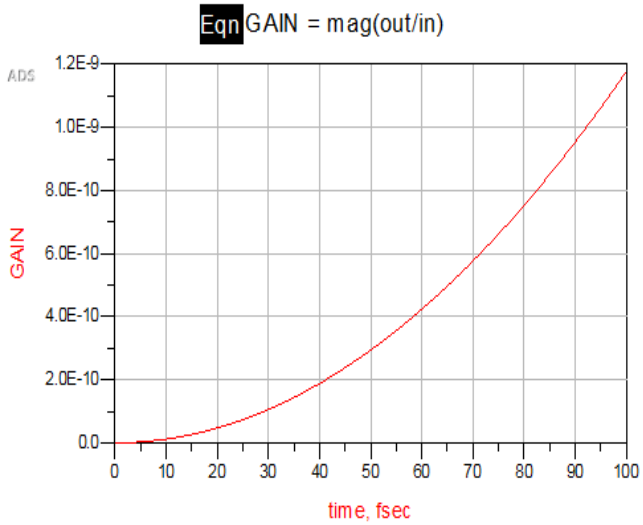

Figure 3

It can be observed that the gain varies linearly with input and time. Sometimes in a power amplifier device gain is not as important as the efficiency and power amplification of the signal.
Following figure shows magnitude of the input with respect to frequency.

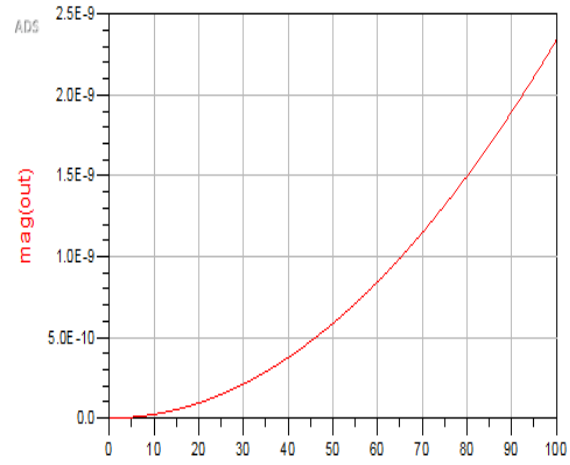

Figure 4

At RF frequencies, Z and Y parameters are not much useful. Therefore for two port networks at RF or mm-wave frequencies Scattering parameters or S-parameters are used. 4 parameters are available for two port networks, namely;

- S_{11}- input voltage reflection constant.
- S_{12}- reverse gain.
- S_{21}- forward gain.
- S_{22}-output voltage reflection constant

Linearity, gain and forward and reverse transmission can be observed by studying these parameters.

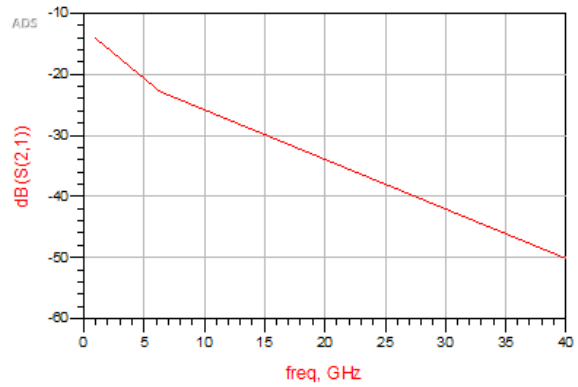

Figure 5

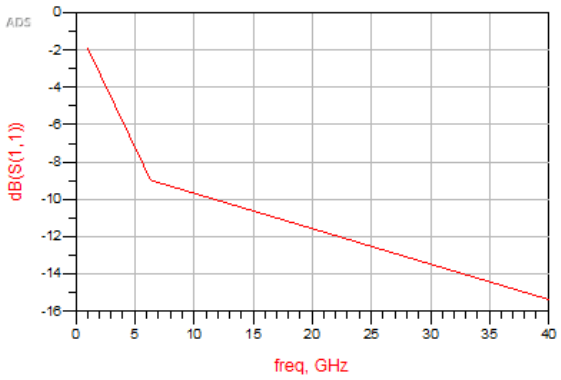

Figure 6

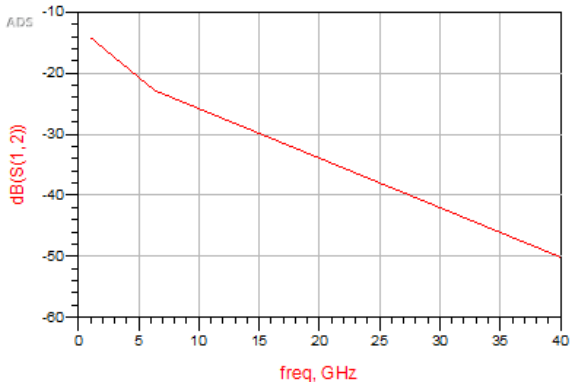

Figure 7

4. CONCLUSION

Common-source topology gives out a better efficiency than cascode however cascode device is more stable at higher frequencies. This is why it is chosen. Proposed device can also be utilized in satellite communication systems. Design shows good linearity with a steady increasing gain. Compression gain of 20dB and PAE of 19% was achieved in the design. Some other matching networks or hybrid networks may also be applied to see if any improvements can be made.

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