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AN OPTIMIZATION POWER OF ADDER TREES FOR MULTIPLE CONSTANT MULTIPLICATIONS

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Abstract

Propagation delays are the major delays caused by the digital circuits and in the data flow graphs (DFG). There are many techniques evolved for reducing the propagation delays. One of them is the retiming process. Retiming, the technique that focuses on inter-changing the delay elements in the flow graph without altering the circuit operation, input and outputs. This method mainly concentrate on the add-multiply blocks i.e. Adders and multipliers. Digital filter uses finite precision for representing signals and are differ from analog filter as digital filter as digital filters uses finite precision arithmetic to compute the filter response. In this project, FIR filter is implemented in Xilinx ISE using VERILOG language . VERILOG coding for the FIR filter is implemented in this project and waveforms are observed through simulation.

Keywords:

Railway track inspection, robot control, train control, gate control, Ultrasonic sensor, Infra-red sensor, GSM,GPS,RF transmitter and receiver

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1. INTRODUCTION

Filter is a frequency selective network. A filter allows a particular band of frequencies and attenuates all the remaining frequencies. Analog and digital are the two types of filter. Depending on the impulse response of a filter it is classified into two types one is finite impulse response and the other is infinite impulse response. The performance of a circuit is implemented by moving the delay elements such as registers and latches without altering its inputs and outputs is known as retiming.

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In this technique, the combinational elements are represented as the vertices of the DFG and the latches are represented as the directed edges. The delay elements of the combinational circuit points correspond to a value. After this, the optimization can be done by interchanging the registers just like bubble pushing. Majorly two operations are used; one is to delete the input vertex after adding a register for all the outputs. The second one is to add the register at input by deleting all the register at the outputs. Whatever the case may be, the functional behavior is not altered.

2. LITERATURE REVIEW

Carry-Save Adder:

The addition of two or more addends is done through carry-save adder. There are many cases where it is desired to add more than two numbers together. Consider the below example

12345678
+87654322
=100000000

Adding process will starts from LSB bits and the result of carry is passed to next bit such that the process goes on until we get the final result and the carry is passed thought the process. A time proportional to n to allow a possible carry to propagate from one end of the number to the other.

1. The addition result is not known
2. The result of addition may be either larger or smaller than the given number
3. The result may be either positive or negative

The major limitation while using Ripple Carry Adder is “carry propagation delay” and this can be overcome when we use “carry look ahead adder”. The delay is reduced by using this adder. But for processing large numbers this adder may also introduces some delay.

Here is an example of a binary sum:

10111010101011011111000000001101
+11011110101011011011111011101111
It computes the sum digit as
10111010101011011111000000001101
+11011110101011011011111011101111
=21122120202022022122111011102212.

3. WALLACE TREE MULTIPLIER:

Adders do not propagate carry to all the bits, so adders are faster than the parallel adders and are widely used to implement the multiplication process. Wallace tree multiplier is one of such circuit that is used to speed up the multiplication process and is made up of combinational logic circuits that are used to multiply the binary integers. General adders like full adder and half adder improves the speed of multiplication process and are essential elements for implementing the multiplication process. Remaining process like ROM look up tables and shift-add approach has an disadvantage that as the number of bits increase the time required to calculate the result linearly increases.

The designed visual inspection robot has been successfully tested on the model track and the detected location has been sent to the phone number which is 2km away from the prototype. This vehicle can be used to detect the track and send GPS coordinates in SMS form to even longer distance provided the GSM signals are intact.

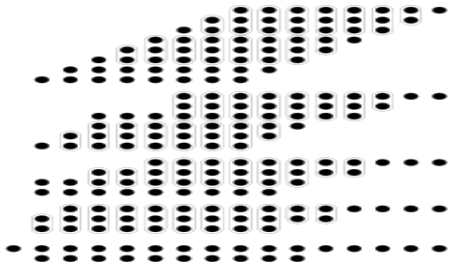


Fig: Wallace Multiplier

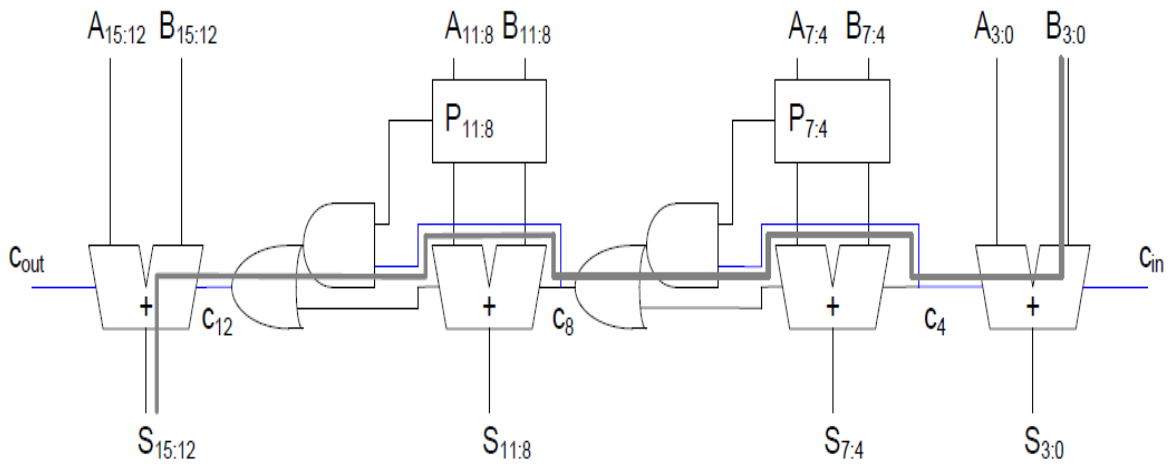
3.2. Wallace Multiplier Operation:

The figure shown above says how to realize Wallace tree multiplier for 8-bit.
The major complexity of many signals processing system is multiplication.
The Wallace multiplier follows below three steps:

1. Full adders are used for calculation of bits in each group.
2. In conventional Wallace reduction single bits are passed to next stage and a group of bits are not processed and they are passed to contrast conventional method.
3. Half adders that are used must known about that stages that shouldn't exceed the number in conventional Wallace multiplier. Half adders are used in final stage of reduction for exceptional cases.

Retiming Adder (carry save adder):

Carry skip adder contains some special blocks that are useful for detecting the bits that are to be added. Here the carry will be either generated or propagated. Carry by-pass adder is also known as carry skip adder. The signal that is produced by this circuit is known as "propagation signal". The carry signal is transmitted through all the stages of blocks and the propagation time is depended on the position of carry that has been generated. If there is no need to calculate the carry then only the time which is required to compute the sum value is considered. The below block diagram has four multiplexers and is considered as 16 bit carry skip adder. The implementation of the circuit is shown below.



4. RESULT AND DISCUSSION

RTL schematic

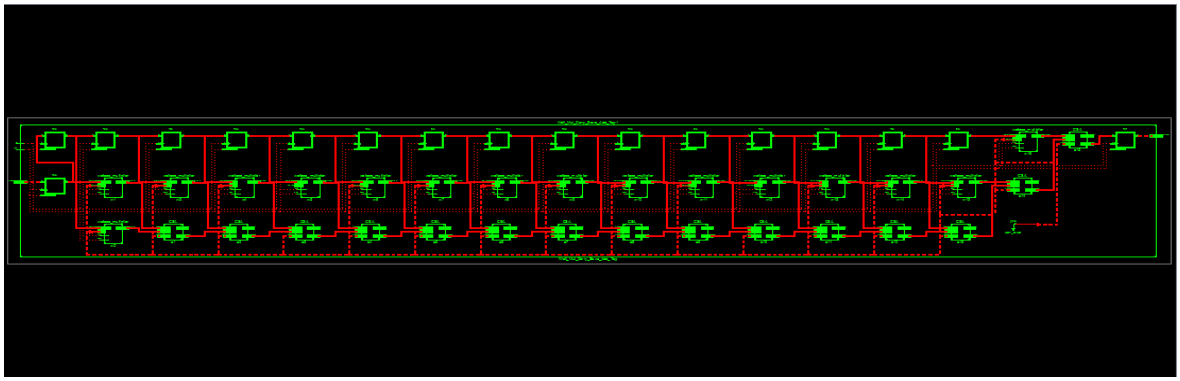


Fig.5: Wallace multiplier with retiming adder

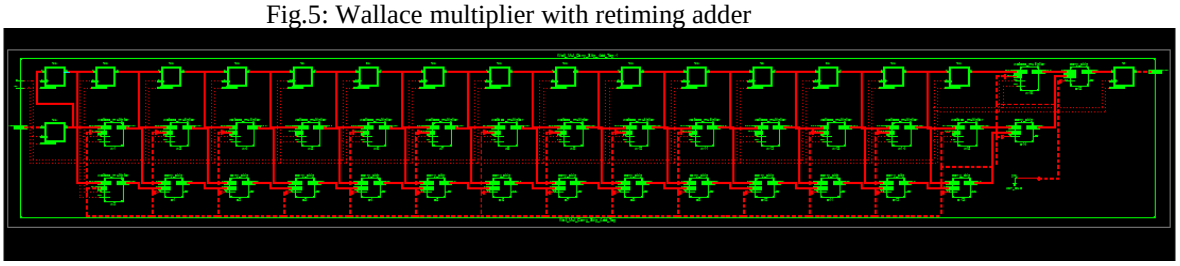


Fig.6: wallace multiplier with carry skip adder

Technological schematics

Fig .7: Wallace multiplier with carry save adder

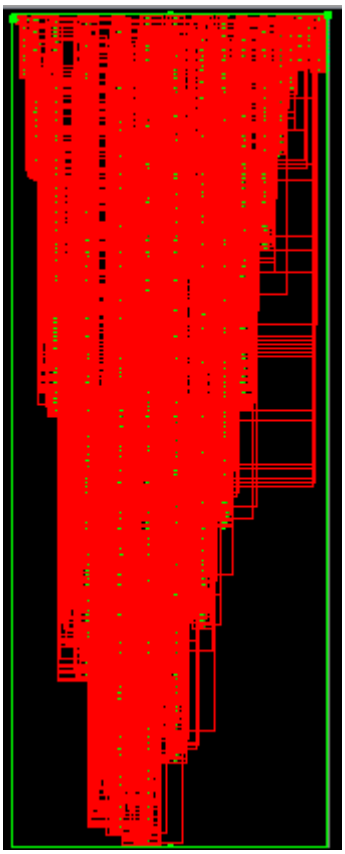


Fig.8: wallace multiplier with carry skip adder.

Wave forms:

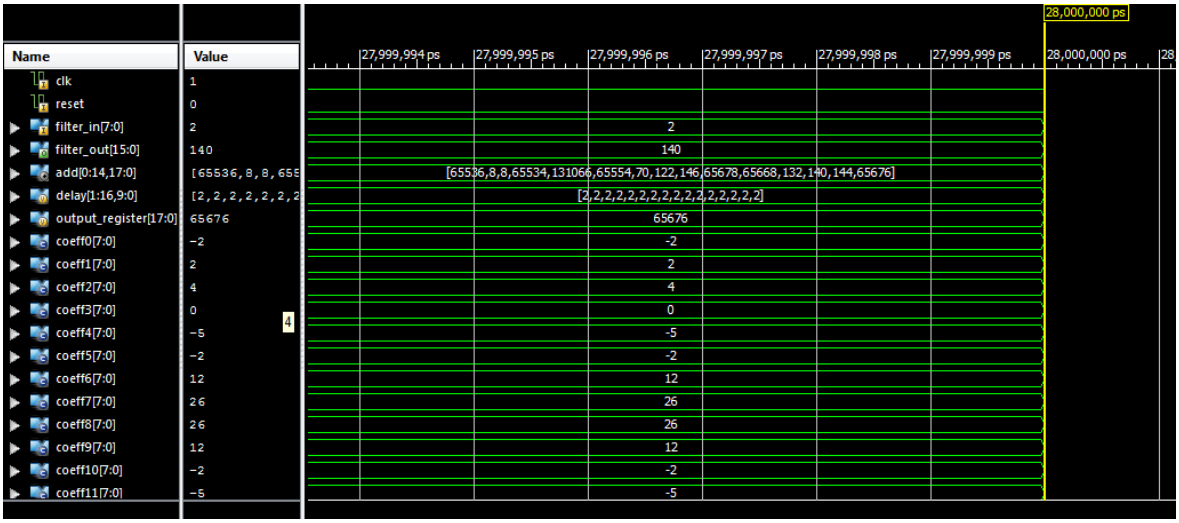


Fig. 9: output's of Wallace with retiming adder.

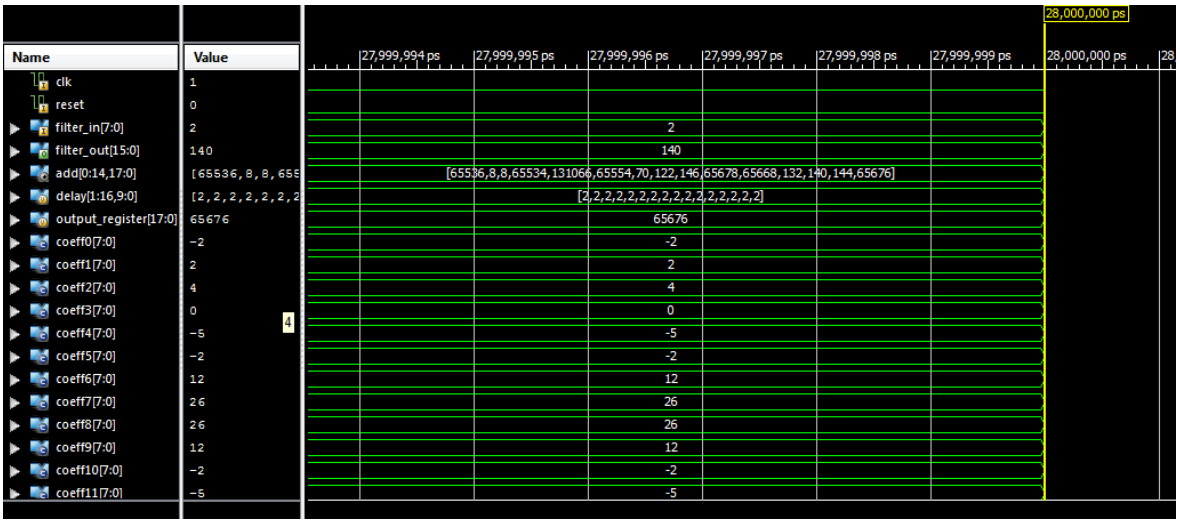


Fig .10: Wallace with carry skip adder.

5. CONCLUSION

In the last two decades, much architecture has been introduced for the design of low complexity fir operation. But there is no such improvement in the FIR design. This project gives the solution for that type of requirements. From the results it can be concluded that the FIR WALLACE CARRY SAVE structure occupies less area, less memory and consumes less power also. But the FIR WALLACE CARRY SKIP structure has less delay when compare with other structures. So from this project it has a chance to use the corresponding structure based on the industrial requirements. In future there may be a chance to develop the layouts for the structures.

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