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A STUDY AND COMPARISON OF VEDIC SQUARE AND MULTIPLIER SUTRA

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ABSTRACT

Square is one of important arithmetic operation. It is used in various signal processing, data analysis. Square can be calculated by using multipliers. Booth algorithm, conventional multiplication and Wallace tree multiplication algorithms are some of multiplier algorithm used while design of multiplier. These algorithms consist of addition of partial products. So, these algorithms are slow. Dedicated square hardware may improve computation time and reduce time delay. Vedic mathematics sutras work on simple principle. Urdhva-tiryagbhyam sutra (UT) is used for multiplication. Yavaduman is used for calculating square. Study of these two sutras and implementation is done using VHDL. In this seminar, analysis of square calculation using UT and Yavadunam sutra had performed.

KEYWORDS:

Urdhva-tiryagbhyam,
Yavaduman,
Booth,Ekadhikina Purvena.
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1. INTRODUCTION

Squaring operation plays very important role in high speed applications. It is special instance of multiplication. Square is the multiplication of the number with itself.

$$X^2=X * X.$$

In most of hardware multiplier units are used to perform square of numbers. There are various multipliers algorithm such as booth, Wallace, array and Vedic etc. Booth algorithm is widely used. It gives procedure of multiplication by using 2's complement.

It consists a lot of steps. So, it requires more time. So, to improve efficiency of multiplication a fast multiplication algorithm is required. A dedicated hardware for square may improve computational efficiency and reduce time. Now days a lot of research is going on Vedic Mathematics. Vedas are store house of knowledge. Vedic Mathematics consist of various sutras. It was rediscovered by Indian mathematician **Jagadguru Shri Bharathi Krishna Tirthaji in** the period between A.D. 1911 and 1918.

This paper is divided into three main sections. Section 1 describes the various Vedic sutras which can be used to calculate square. Section 2 consist of simulation results, while section 3 consists conclusion.

Section 1

2. VEDIC SUTRAS

There are 16 sutras in Vedic Math's. It provides easy way to solve problems of algebra, geometry, calcus.Urdhva – tiryagbhyam is sutra used for multiplication. Urdhva – tiryagbhyam means vertical and crosswise operations. It is faster than other multiplier algorithms. Ekadhikena Purvena, Yavadunam, Dwandwa Yoga, Urdhva-tiryagbhyam sutras are used for Square calculation.

2. 1 Urdhva Tiryagbhyam

Urdhva Tiryagbhyam (Vertical and Crosswise): It is one of the sutras in Vedic mathematics. The main goal is to reduce the delay It is used for multiplication. As square is special case of multiplication. This multiplication algorithm can be used for calculating square. Now a days it is used for designing MAC unit. Hierarchical approach is used while designing 32-bit UT multiplier. Initially 2 X 2 Vedic multiplier is designed. By using 2 x 2 Vedic multiplier 4 X 4 Vedic multiplier is designed. In such way larger bit multiplier is designed.

Two half adders are used for designing 2 X 2 Vedic multiplier.

Consider A and B are two-bit binary number. The result of multiplication is stored at Y. C has been used for expressing carry. Mathematical expression of two-bit Vedic multiplier is as below:

C0 Y0=A0 X B0
C1Y1=A1 X B0+ B1 X A0+C0
C2Y2=A1 X B1 +C1
Answer: C2Y2Y1Y0

Block Diagram of two-bit Vedic Multiplier is below:

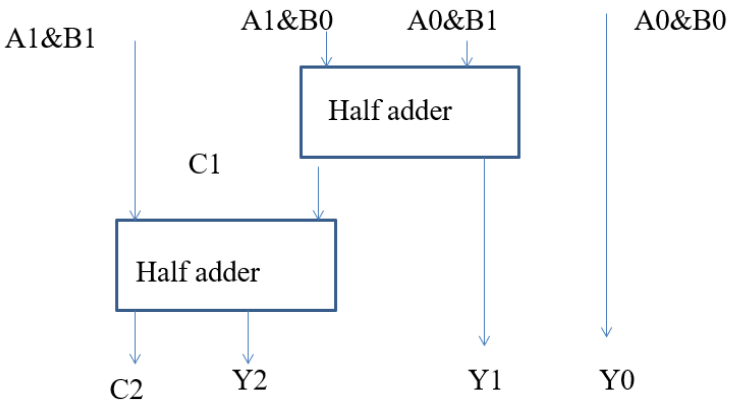


Figure 1. *Block Diagram of Two-bit Vedic Multiplier*

Example of 2-bit binary number multiplication using Urdhva-Tiryagbhyam sutra is explained along with calculation as below.

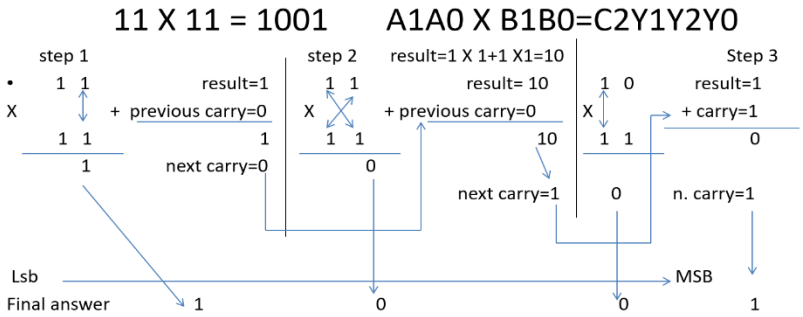


Figure 2.*Example of Two bits vedic multiplication*

There is pattern in the vertical and crosswise multiplication and addition . It varies with increase number of bits. With help of 2-bit four-bit Vedic multiplier is made. Two-bit Vedic multiplier can be designed by using and gates and two half adders. A four-bit Vedic multiplier is designed by using 4 two-bit multiplier blocks and 3 ripple carry. Here a 4 bits Vedic multiplier along with inputs a and b has shown in fig. 2. Output is observed at Y which is of eight bits.

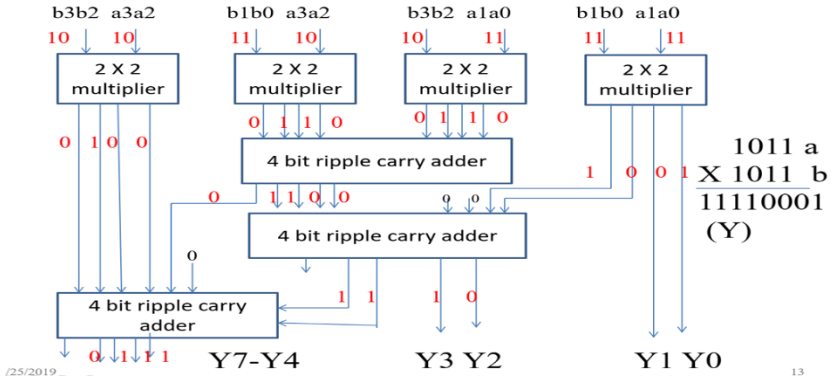


Figure 3.*Example of Four bits vedic multiplication*

While 8-bit Vedic multiplier is designed to perform the analysis of delay and resource utilization. Vedic multiplier is compared with booth multiplier. It is designed by using four-bit multiplier and adder [5].

2.2 Yavadunam

Yavadunam Sutra is one of the squaring sutras of Vedic mathematics [1]. It increases a speed of square calculation. It compares a number with respect to base value. For N bit binary number, the base value is $2^{(N-1)}$. Eight is base value for four-bit binary number. Deficiency calculated by subtracting number from its base value. It operates in two modes. If four-bit binary number is greater or equal than 8 then mode 1 is selected else mode 2 is selected. Output of mode 1 is of eight bits. While output of mode 2 is of six bits.

Mode: 1 The given number is greater than $2^{(N-1)}$.

Mode: 2 The given number is lesser than $2^{(N-1)}$.

Example: For a four-bit Yavadunam sutra, input number is 3

Base Value:8

Deficiency:8-3=5

As input number (3) < 8, mode 2 is selected

Let consider P as four-bits binary input. According to the value of input Modes are selected. If P is greater than or equal to 8 then output is Q. If P is less than 8 then output is observed at

R. Q and R are output ports of eight bits and six bits.

Algorithm for Mode 1

INPUT: P3P2P1P0

OUTPUT: Q7. . . Q2Q1Q0

Step:1) Calculate deficiency by removing MSB bit of input.

Step:2) Deficiency is denoted by D. It has three bits as D2D1D0. Deficiency is calculated as D2D1D0 = P2P1P0

Step:3) Square the deficiency, output of squaring=X5. . . X2X1X0

Carry = X5X4 X3 and now

LHS =X2X1X0 = Q2Q1Q0

Step:4) Add the deficiency and the input [1]

P3P2P1P0 + D2D1D0 = Y4Y3Y2Y1Y0

Step:6) Add the above output to the carry of the LHS [1]

Y4Y3Y2Y1Y0+ X2X1X0 = Q7Q6Q5Q4Q3 =RHS

Step:7) Square of input number is given by combiningLHS and RHS [1]square of P3P2P1P0= Q7Q6Q5Q4Q3Q2Q1Q0

Algorithm for Mode: 2

INPUT: P3P2P1P0

OUTPUT: R5. . . R2R1R0

Step:1) Reduce the weight of the input by removing the MSB,now input becomes P2P1P0.

Step:2) Take two's complement of P2P1P0, the output is the deficiency. Let the deficiency be

D2D1D0 = P2P1P0

Step:3) Square the deficiency, output of squaring=X5. . . X2X1X0

Carry = X5X4 X3 and now

LHS =X2X1X0 = R2R1R0

Step:4) Subtract the deficiency from the bit reduced number P2P1P0 - D2D1D0 = Y2Y1Y0

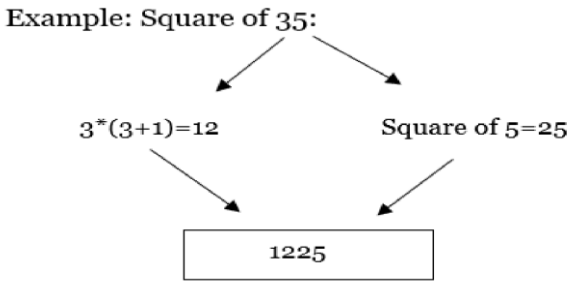
Step:5) If the subtractor output is positive then add the above output to the carry X5X4 X3. Y2Y1Y0 + X5X4X3 = R5R4R3 =RHS

Step:6) If the subtractor output is negative then subtract the output Y2Y1Y0 from the carry X5X4X3. i.e. X5X4X3 - Y2Y1Y0 = R5R4R3 =RHS

Step:7) Concatenating LHS and RHS, the output is R5R4R3R2R1R0 =square of P3P2P1P0

2. 3 Ekadhikina Purvena

This sutra Ekadhikina Purvena means, By one more than the previous". This sutra can be used to find the square of numbers with the specification condition that the number to be squared
has the 5 as last digit.
Eg:2935, 98274635, 5, 895, ….



Example of Square

The above method had explained simple approach to calculate square of number with unit place 5.

Section II

3. Simulation Results of Vedic Sutra

VHDL is one of hardware descriptive language Xilinx ISIM software is used to design hardware for Yavadunam and Urdhva Tiryagbhyam Vedic Sutra. Xilinx release version on 14.7 has been used.

3.1 Yavadunam Sutra for four bits:

Here a is input and the output is observed at b and c. If p is greater than or equal to 8 then output is observed at q. If p is less than 8 then output is observed at r:

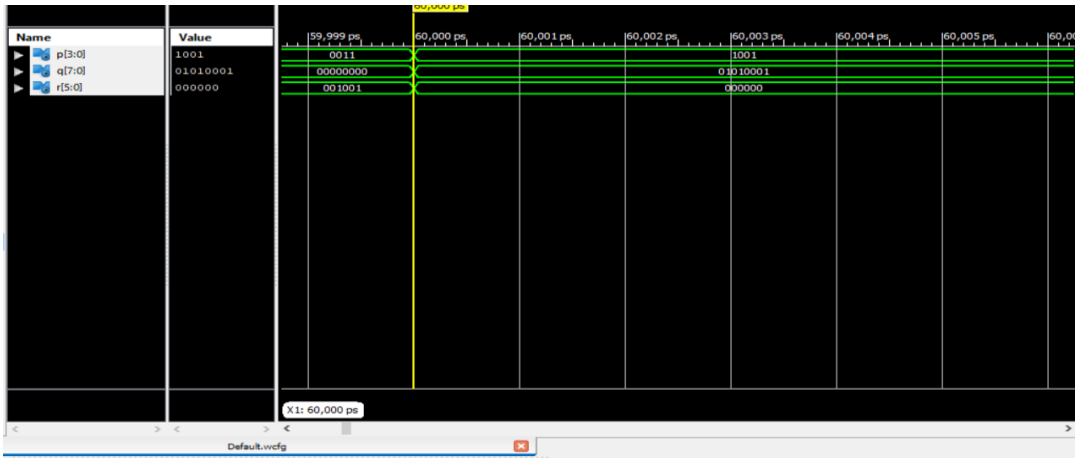


Figure 4.*Yavadunam Square Output*

RTL design of Yavadunam Square is as Follows:

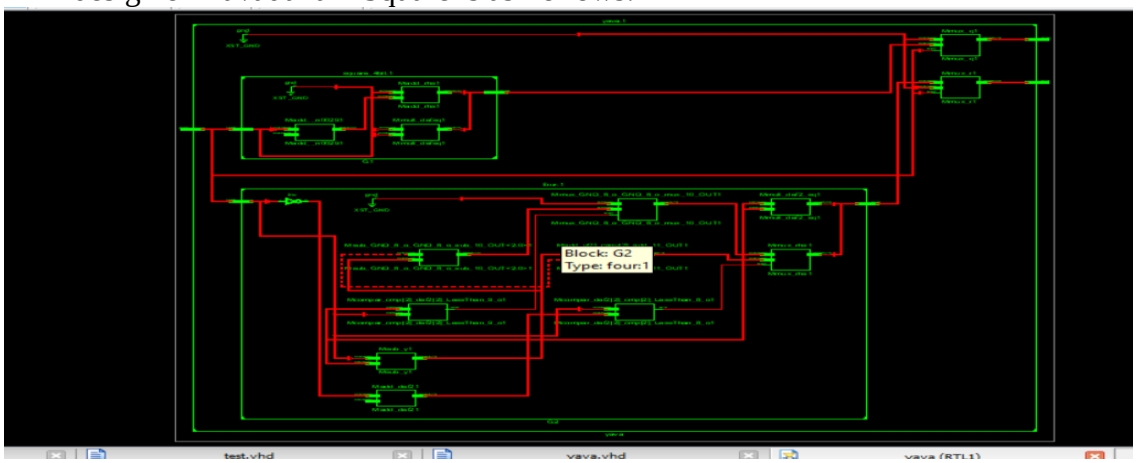


Figure 5. *RTL of Yavadunam Square*

From the analysis of synthesis report of design, the table is prepared. It consists details about LUT utilization, delay, number of IO of the design. The table is as follows

Table 1. Analysis of Yavadunam

Parameters	Values
Number of slices of LUT used	12
Number of IO	18
Delay in ns	5.731

3.2 Urdhva Tiryagbhyam Sutra for four bits

Four bits Vedic Multiplier is designed by using four 2-bit s Vedic multiplier and four-bits ripple carry adder.

Here x and y are multiplier and multiplicand, while output is observed at Mult(Variable).

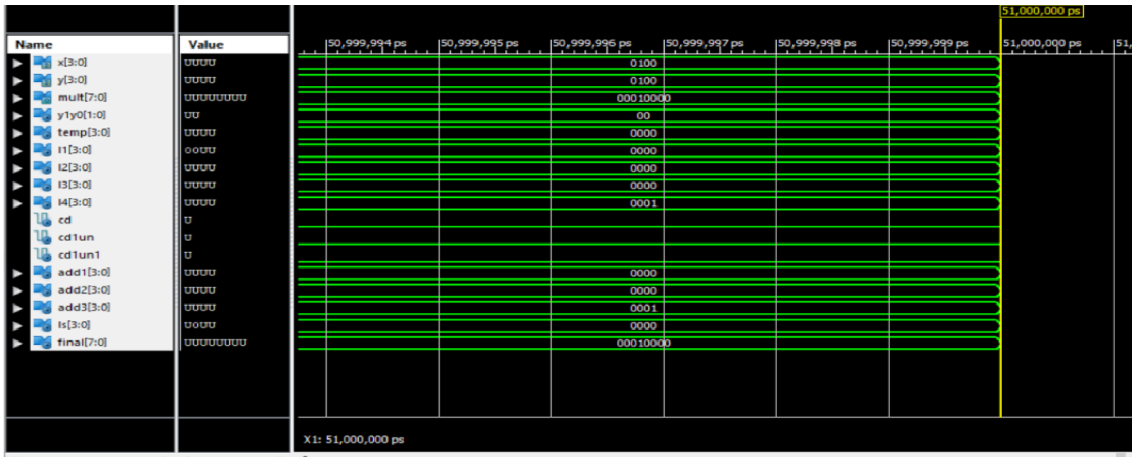


Figure 6. *Simulation result of 4-bits Urdhva-Triyabhagam sutra*

RTL design of four-bits Urdhva-Triyabhagam as below:

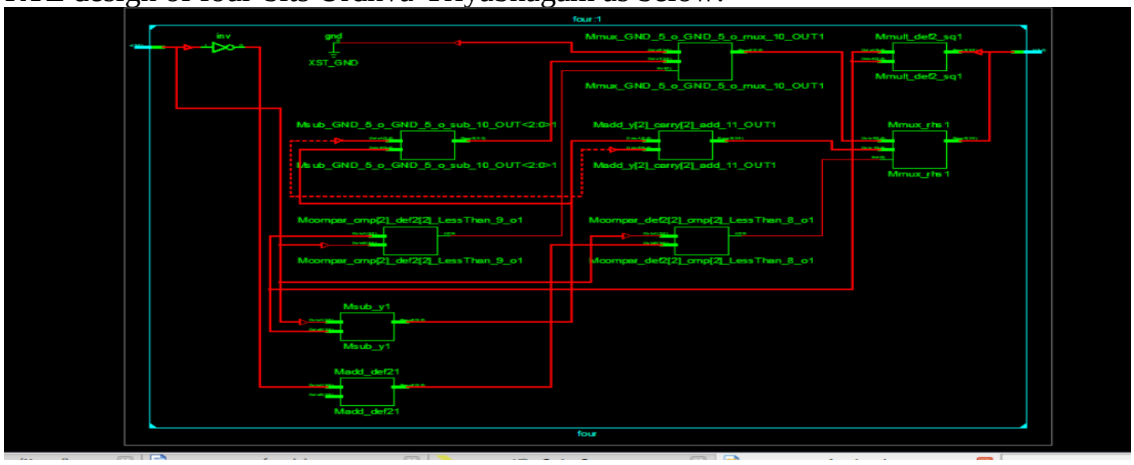


Figure 7. *RTL of 4 Bit Urdhva Tiryagbhyam Sutra*

From the analysis of synthesis report of design, the table is prepared. It consists details about LUT utilization, delay, number of IO of the design. The table 2 is as follows:

Table 2. Analysis of Urdhva Tiryagbhyam

Parameters	Values
Number of slices of LUT used	24
Number of IO	16
Delay in ns	11.448

4. CONCLUSION

Delay is one of the measuring parameters of performance. If a delay of design is less that means the design is fast. Slower design will have high delay. From the above simulation results, we can conclude that Urdhva-Tiryagbhyam is faster than booth algorithm. Vedic multiplier are even simple to design than complex booth multiplier algorithm. Vedic multiplier are very efficient than other multiplier as far as delay is concern. Speed of Yavadunam sutra is get improved by using bit reduction method. Yavadunam sutra performs square calculation faster than Urdhva-Tiryagbhyam sutra. It is also seen that as design style varies the results such IO utilization and memory utilization is varying. But the delay is getting reduced as expected.

A dedicated hardware will improve the system performance but may leads to the area overhead.Square sutra is faster than the Vedic multiplier sutra. From synthesis report analysis of comparison of Vedic UT sutra and Yavadunam sutra.

Table 3. Comparison between square usingUT and Yavadunam sutra for four bits

Method	Total delay (ns)	No. of LUT
Urdhva-tiryagbhyam (UT)	11.448	24
Yavadunam	5.731	12

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